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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,616	03/09/2001	Yatin V. Hoskote	2207/10554	7643

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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,616	HOSKOTE ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been presented for examination based on applicant's request for reconsideration filed on 10 January 2005. Claims 1-21 remain rejected by the examiner.

Response to Arguments

2. Applicant's arguments filed 10 January 2005 have been fully considered but they are not persuasive.

Regarding applicant's response to 102(b) rejection: The thrust of applicant's arguments center around arguing that the prior art (Burch) does not teach detecting the "polarity" of the mappings in an inversion detection phase. The examiner notes that Figure 6 of applicant's specification appears to indicated the claimed "inversion detection phase" merely consists of detecting that latch outputs Z and Z' are of "opposite" values. This observation is supported by the passages recited on page 10, line 9 of applicant's specification. In this case, the claimed "polarity" is simply the latch state (or opposite state) for any given simulation and the "inversion diction phase" merely determines "opposite output" values. The examiner has asserted that Burch teaches a functionally equivalent process. Specifically, as referenced in the examiners office action, Burch teaches a method for automatically mapping state elements inclusive of recombining the latch states from a combined state via a transitions state (CL3-L33-CL5-L5, Figs. 6, 7). This includes a refinement process that assumes both true and false latch output values in the mapping process. (CL4-L57-67) That is,

the "polarity", or an "opposite" true/false value, in any latch output would inherently be detected in recombining of the latch states disclosed by Burch. Applicants have merely argued that the prior art does not teach an inversion detection phase but not specifically argued how the claimed inversion detection is distinguished over the cited prior art.

Regarding 103(a) rejections motivation to combine: The examiner contends that the motivation to combine Burch and Lin is proper and in accordance with MPEP guidelines for the following reasons. MPEP 2143.01 Suggestion or Motivation To Modify the References first recites:

"There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art." In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998)

Therefore, in suggesting a motivation to combine, the examiner specifically focused his motivation on the knowledge of persons of ordinary skill in the art. More specifically, that a skilled artisan would have made an effort to become aware of what capabilities had been developed in the market place, and hence would have knowingly modified Burch with the teachings of Lin. (See: office action pages 8-9) MPEP 2144 Sources of Rationale Supporting a Rejection Under 35 U.S.C. 103 recites:

"The rationale to modify or combine the prior art does not have to be expressly stated in the prior art; the rationale may be expressly or impliedly contained in the prior art or it may be reasoned from knowledge generally available to one of ordinary skill in the art, established scientific principles, or legal precedent established by prior case law. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). See also In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) (setting forth test for implicit teachings); In re Eli Lilly & Co., 902 F.2d 943, 14 USPQ2d 1741 (Fed. Cir. 1990) (discussion of reliance on legal precedent); In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988) (references do not have to explicitly suggest combining teachings)"

The examiner has simply asserted that a skilled artisan tasked with solving the problem of determining mappings between state elements of a first and second circuit (i.e. as taught by Burch), and determining fan-in and fan-out sets of combinational components (i.e. as taught by Lin), and further having access to the teachings of Burch and Lin, would have knowingly modified the teachings of Burch, with the teachings of Lin in order to gain the advantage of reduced cost and development time. Specifically, a skilled artisan working in this obviously competitive environment would have made an effort to become aware of what capabilities had already been developed in the market place, and hence would have been aware of, and known to seek out the relative teachings of the problem to be solved. Namely, the teachings of Burch and Lin.

MPEP 2143.01 Suggestion or Motivation To Modify the References further recites the following supporting rational:

> Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. **"The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art."** In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

The examiner therefore appears to have established an implicit showing that in view of the combined teachings of the prior art, the relative knowledge of one skilled in the art, and in particular, the nature of the problem to be solved, there exists an obvious motivation to combine the references as noted in the 103(a) rejection below.

For the reasons set forth above the examiner maintains the 102(b) and 103(a) rejections.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,247,163 issued to Burch et al.

Independent claims 1, 18, and 20 are drawn to:
Method for mapping state elements between first and second circuit by:
Comparing state element features (structural phase) in first circuit to second
Determining mappings between state elements in first and second circuit
Accounting for "don't care" conditions before comparing before comparing
Detecting polarity (inversion detection) of mappings
Comparing state element (functional phase) equivalence by three-valued simulation
Determining further mappings from functional phase
Detecting threshold condition for completion

Regarding independent claims 1, 18, and 20: Burch discloses the elements of the claimed limitations of the present invention as follows:

- Method for mapping state elements between first and second circuit: Burch discloses the mapping of state (latch) elements between a first and second circuit (Abstract, Summary of Invention, CL12-L14, 44, Figs. 5-8B)

- Comparing state element features (structural phase) in first circuit to second: Burch discloses comparing (determining correspondence) between a first and second circuit (CL9-L17-CL10-L33, CL11-L3-10, 29-35, Figs. 5-8B). The examiner has interpreted this process to be functionally equivalent to the structural phase of the claimed invention that compares element features between a first and second circuit.

- Determining mappings between state elements in first and second circuit: Burch discloses determining mappings between state elements of a first and second circuit (CL7-L38, CL11-L35-38, Figs. 5-8B).

- Accounting for "don't care" conditions before comparing before comparing: Burch considers don't care conditions in mapping state elements (Abstract, CL2-L53, CL9-L17, Figs. 5-8B).

- Detecting polarity (inversion detection) of mappings: Burch discloses inversion detection of combined state element mappings (CL3-L33-CL5-L5).

- Comparing state element (functional phase) equivalence by three-valued simulation: Burch considers equivalence of three state values (CL12-L14, 44).

- Determining further mappings from functional phase: Burch performs further mapping after considering equivalence (CL9-L17-CL10-L33, CL11-L39-44).

- Detecting threshold condition for completion: Burch discloses a completion condition (Fig. 8B, 870).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 2-17, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,247,163 issued to Burch et al in view of U.S. Patent 6,651,225 issued to Lin et al.

Regarding independent claims 1, 18, and 20: As cited previously, Burch discloses the elements of the claimed limitations of the present invention as follows:

- Method for mapping state elements between first and second circuit: Burch discloses the mapping of state (latch) elements between a first and second circuit (Abstract, Summary of Invention, CL12-L14, 44, Figs. 5-8B).

- Comparing state element features (structural phase) in first circuit to second: Burch discloses comparing (determining correspondence) between a first and second circuit (CL9-L17-CL10-L33, CL11-L3-10, 29-35, Figs. 5-8B). The examiner has interpreted this process to be functionally equivalent to the structural phase of the claimed invention that compares element features between a first and second circuit.

- Determining mappings between state elements in first and second circuit: Burch discloses determining mappings between state elements of a first and second circuit (CL7-L38, CL11-L35-38, Figs. 5-8B).

- Accounting for "don't care" conditions before comparing before comparing: Burch considers don't care conditions in mapping state elements (Abstract, CL2-L53, CL9-L17, Figs. 5-8B).

- Detecting polarity (inversion detection) of mappings: Burch discloses inversion detection of combined state element mappings (CL3-L33-CL5-L5).

- Comparing state element (functional phase) equivalence by three-valued simulation: Burch considers equivalence of three state values (CL12-L14, 44).

- Determining further mappings from functional phase: Burch performs further mapping after considering equivalence (CL9-L17-CL10-L33, CL11-L39-44).

- Detecting threshold condition for completion: Burch discloses a completion condition (Fig. 8B, 870).

Burch does not explicitly disclose elements relating to determining equivalence between circuits based on fan-in and fan-out (equivalence) in mapping state elements as recited in the limitations of dependent claims 2-17.

Per dependent claims 2-17, 19, and 21: Lin discloses determining fan-in and fan-out sets of combinational components (elements) that the examiner has equated to be functionally equivalent to the fan-in and fan-out signatures of the claimed invention. (Lin: CL58-L39-CL60-L13, Fig. 16) The limitations relating to parallel comparisons (claims 10, 11) are inherently disclosed by Burch since the equivalence comparisons cited above are performed between two circuits simultaneously. (Burch: CL9-L17-CL10-L33, CL11-L3-10, 29-35, Figs. 5-8B) Burch also discloses inputting random values during equivalence comparisons as recited in the limitations of claims 6, 13, 14, 19, and 21. (Burch: Abstract, Summary of Invention, Fig. 3A)

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings Burch relating to determining mappings between state elements of a first and second circuit, with the teachings of Lin relating to determining fan-in and fan-out sets of combinational components (elements), to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many types of equivalence verification process available for VLSI circuit development in the market place and large amounts of money being spent in product development and improvement. (see U.S. 6,496,955 Background for example) Accordingly, a skilled artisan would have made an effort to become

aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Burch with the teachings of Lin in order to reduce development time and cost.

Conclusion

5. ***THIS ACTION IS MADE FINAL.*** *Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,496,955 issued to Chandra et al discloses mapping of component elements in equivalence verification.

U.S. Patent 6,035,109 issued to Ashar et al discloses mapping of component elements in equivalence verification.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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May 19, 2005

JEAN R. HOMERE
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